REMARKS

35 U.S.C. Section 102 Rejections

The above referenced Office Action states that Claims 1-5 and 13-17 are rejected as allegedly being anticipated by Ma (US Patent No. 6320437). Applicant has amended independent Claims 1, 7, 13, and 19 to more particularly point out aspects of the present invention. Dependent Claims 4, 10, 16, 22, and 24 have been cancelled. Applicant respectfully asserts that the claimed embodiments as recited in the newly amended independent Claims 1, 7, 13, and 19 are not anticipated by the Ma reference.

The Ma reference discloses a duty cycle regulator circuit that derives an output clock signal having an adjustable duty cycle from a single input clock signal. The cited "clock pulse generator 30" of Figure 2 of Ma receives the input clock signal "CLK_IN 33" and generates therefrom a set signal for the "clock output unit 10." Importantly, this is the only signal received by the clock pulse generator 30 to create the signals for the clock output unit 10. The reset signal is generated from the output of the clock pulse generator 30. The reset signal for the clock output unit 10 is described as a pulse provided by buffers of a delay circuit. As such, the reset signal does not comprise a second input, but is merely a delayed version of the output of the clock output unit 10.

In contrast, each of the independent claims of the present invention have been amended to explicitly recite an edge detection circuit configured to receive an external clock signal and generate an output therefrom and a conditioning circuit for producing a conditioned signal having a one half clock period delayed phase with respect to the external clock signal (emphasis added). Thus, in Claim 1 for example, the latch circuit uses two inputs, one from the edge detect circuit that yields the rising edge of the internal clock signal and one from the conditioned signal that yields the falling edge of the internal clock signal. The conditioned signal used by the latch does not come from the output of the latch circuit

(e.g., the "internal clock signal"). The conditioned signal is not a delayed version of the output of the latch circuit.

This is completely different from Ma, where the reset signal is explicitly disclosed as being generated from the output of the "clock output unit 10" of Ma. Thus, Applicant respectfully asserts that the present invention as recited in the amended independent Claims 1, 7, 13, and 19 is not anticipated by the Ma reference within the meaning of 35 U.S.C. Section 102.

35 U.S.C. Section 103 Rejections

Claims 7-12 and 19-24 are rejected under 35 U.S.C. § 103 as being rendered unpatentable by Ma in view of Huynh (U.S. Publication No. 2003/0107432). Applicant has amended independent Claims 1, 7, 13, and 19 to more particularly point out aspects of the present invention. Applicant respectfully asserts that the present invention as recited in newly amended independent Claims 1, 7, 13, and 19 is not rendered unpatentable by Ma and Huynh within the meaning of 35 U.S.C. § 103.

As described above, the independent claims of the present invention have been amended to explicitly recite an edge detection circuit configured to receive an external clock signal and generate an output therefrom and a conditioning circuit for producing a conditioned signal having a one half clock period delayed phase with respect to the external clock signal (emphasis added). These limitations are not shown or suggested by the Ma reference.

The addition of the Huynh reference does not cure the shortcomings of Ma. Huynh is relied upon to show a switched capacitor component of an ADC (Analog to Digital Converter). The cited combination does not show or suggest a latch circuit using two

inputs, one from the edge detect circuit that yields the rising edge of the internal clock signal and one from the conditioned signal that yields the falling edge of the internal clock signal. The cited combination does not show or suggest a VCRO input used in conjunction with the edge detect circuit (e.g., as in independent Claims 13 and 19). These limitations are not shown or suggested by the cited combination. Accordingly, the cited combination does not render the present invention obvious as recited in independent Claims 1, 7, 13, and 19 within the meaning of 35 U.S.C. Section 103.

CONCLUSION

For the reasons discussed above, Applicant respectfully asserts that the 35 U.S.C. § 102 rejections and 35 U.S.C. § 103 rejections are overcome. Applicant respectfully submits that all remaining claims (Claims 1-3, 5-9, 11-15, 17-21, and 23) of the present application are now allowable.

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,
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